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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,501	06/30/2003	Terry L. Sterrett	42P15934	3363

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/611,501	STERRETT ET AL.	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 15* is/are pending in the application.

4a) Of the above claim(s) *12 - 15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on June 13, 2005 has been received and entered in the case.

Response to Affidavit 37 CFR 1.131

2. The affidavit filed on June 13, 2005 under 37 CFR 1.131 is sufficient to overcome the Mistry et al. (U.S. Pat. No. 6,815,254) reference.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1 – 7 and 9 – 11 are rejected under 35 U.S.C. 102(b) as being anticipated by Takahashi et al. (U.S. Pat. No. 6,287,892).

Regarding claim 1, Takahashi et al. discloses in e.g., Fig. 2 an apparatus comprising:

- a first support substrate (1, at the middle; column 3, lines 60 and 61)comprising a plurality of first support contacts (4; column 3, line 61) and a plurality of second support contacts (5; column 4, line 11) on a surface of the first support substrate;
- a chip (2; column 3, line 62) comprising a plurality of circuits (circuits in the active area of the chip that connect the chip pads or interconnect layers of the chip to the

chip contacts) coupled to respective ones of a plurality of externally accessible chip contacts (at the areas on the chip that are connected to the bump 3; column 3, line 62), wherein the chip contacts are coupled (by bump 3) to respective ones of the first support contacts (4; see e.g., Fig. 2);

- a plurality of fusible masses (7; column 4, lines 12 – 19) coupled to respective ones of the plurality of second support contacts (5; see e.g., Fig. 2);
- an electrically-insulating encapsulant (8; column 4, lines 28 – 32 and lines 61 – 65) on the first support substrate and the chip; and
- a second substrate (1, at the top; column 3, lines 60 and 61);
- wherein the encapsulant (8) is disposed between and contacts the first support substrate and the second support substrate (see e.g., Fig. 2).

Regarding claim 2, Takahashi et al. discloses in e.g., Fig. 2 the plurality of fusible masses (7) having a thickness at least equivalent to the thickness of the encapsulant measured from the surface of the first support substrate at one of the plurality of fusible masses (column 4, lines 15 – 19).

Regarding claims 3 and 10, Takahashi et al. discloses in e.g., Fig. 2 the encapsulant (8) being present in an amount to encapsulate the chip (2), circuit structure (claim 10; wiring pattern; column 3, line 61) and encapsulating a portion of respective ones of the plurality of fusible masses (7; see e.g., Fig. 2).

Regarding claim 4, Takahashi et al. discloses in e.g., Fig. 2 the plurality of second support contacts (5) being positioned on the first support substrate to align with contacts (5, at

the bottom surface of the top substrate 1) of the second support substrate (1, at the top; see e.g., Fig. 2).

Regarding claim 5, Takahashi et al. discloses in e.g., Fig. 2 the plurality of second support contacts (5) being positioned around the periphery of the first support substrate.

Regarding claim 6, Takahashi et al. discloses in e.g., Fig. 2 the second support substrate (1, at the top) comprising a plurality of second support contacts (5, at the bottom surface of the top substrate 1) on a surface thereof, the plurality of second support contacts coupled directly to respective ones of the plurality of fusible masses (7).

Regarding claim 7, Takahashi et al. discloses in e.g., Fig. 2 an apparatus comprising:

- a first support substrate (1, at the middle) comprising at least one circuit structure (2) and a plurality of first support contacts (5) on a first surface thereof, the plurality of first support contacts electrically coupled (by bump 3 and wiring patterns; column 3, lines 60 – 64) to respective ones of circuits (pads on the chip 2) of the at least one circuit structure (2, at the middle);
- a plurality of fusible masses (7) on respective ones of the plurality of first support contacts;
- an electrically-insulating encapsulant (8) on the first support substrate and on the at least one circuit structure; and
- a second support substrate (1, at the top) comprising at least one circuit structure (2, at the top) on a first surface thereof and having a plurality of second support contacts (5, at the bottom surface of the top substrate 1) on a second surface thereof and coupled to respective ones of the plurality of fusible masses (7), the plurality of

second support contacts electrically coupled to respective ones of circuits of the at least one circuit structure (2, at the top; see e.g., Fig. 2),

- wherein the encapsulant (8) is disposed between and contacts the first support substrate and the second support substrate (see e.g., Fig. 2).

Regarding claim 9, Takahashi et al. discloses in e.g., Fig. 2 the plurality of fusible masses (7) having a thickness at least equivalent to the thickness of the encapsulant (8) measured from the surface of the first support substrate at one of the plurality of fusible masses (column 4, lines 15 – 19).

Regarding claim 11, Takahashi et al. discloses in e.g., Fig. 2 the plurality of support contacts (5) of the first support substrate being positioned around the periphery of the first support substrate.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. in view of Chatterjee (U. S. Pat. No. 4,695,872).

While Takahashi et al. discloses in Fig. 6 the use of chips or circuit structures in each one of the chip packages, Takahashi et al. does not appear to provide a specific type of the at least

one chip to be a microprocessor and the other chip to be a memory. Chatterjee teaches in e.g., Fig. 4 and column 3, lines 63 – 64 at least one chip (14) to be a microprocessor on a first support substrate (10) and the other chip to be a memory (16) on a second support substrate (52). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to apply the microprocessor chip and memory chip as the specific type of the chips of Takahashi et al. as taught by Chatterjee to provide high speed exchanges of data between the memories to perform a task according to a software program (column 2, lines 1 – 6).

Response to Arguments

7. Applicant's arguments with respect to claims 1 and 7 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Friday, June 17, 2005

GEORGE ECKERT
PRIMARY EXAMINER